[0026] FIG. **5** illustrates an equivalent circuit diagram of the structure shown in FIGS. **3**A through **3**C, wherein drain region **20**, source regions **126** and **26**, and gates **24** and **48**, of MOS transistor **62** and JFET **300**, respectively, are marked. By integrating MOS transistor **62** and JFET **300**, the chip area that is used by integrated MOS transistor **62** and JFET **300** in combination may be reduced.

[0027] FIG. **4**A illustrates a top view of JFET **400**. JFET **400** has a similar top view as that of JFET **300** in FIG. **3**, except that PW region **40** is separated into PW regions **40**A, **40**B, and **40**C, which are spaced apart from each other by the separated portions of HVNW regions **38**. Insulation region **46'** (Please refer to FIGS. **4**B and **4**C) is formed over HVNW region **38** to separate PW region **40**A from PW region **40**B.

[0028] Again, MOS source region **126**, gate electrode **24**, and drain **20** form the source region, the gate, and the drain region, respectively of MOS transistor **62**. Drain region **20** acts as the drain region of both MOS transistor **62** and JFET **400**. On the other hand, PW pickup regions **48**B and **48**C are interconnected to act as the gate of JFET **400**. The pinch-off and the turning-on of JFET **400** may be achieved by applying appropriate voltages to PW pickup regions **48**B and **48**C. When turned on, JFET **400** has current I**1** (FIGS. **4**B and **4**C) that flows under PBL **42**, and flows to the source region **26** of JFET **400**. Current I**1** is illustrated in FIGS. **4**B and **4**C, which are cross-sectional views obtained from the plane crossing lines **4**B-**4**B and **4**C-**4**C, respectively, in FIG. **4**A. An equivalent circuit diagram of the structure in FIGS. **4**A through **4**C is also illustrated in FIG. **5**.

[0029] In the embodiments, the pinch-off voltages of the JFETs may be easily adjusted by adjusting the channel width, such as the distances between PW regions **40**. The embodiments also provide a solution for a high-voltage JEFT design, with the drain voltage of the JFETs in accordance with embodiment being higher than about 400 V. Due to the use of the 3D channels (for example, referring to currents I**1** and I**2** in FIGS. **1**B and **1**C), the turn-on resistance of the JFETs is low.

[0030] In accordance with some embodiments, a device includes a buried well region of a first conductivity type over the substrate, and a first HVW region of the first conductivity type over the buried well region, an insulation region over the first HVW region. A drain region of the first conductivity type is disposed on a first side of the insulation region and in a top surface region of the first HVW region. A gate electrode includes a first portion on a second side of the insulation region, and a second portion extending over the insulation region. A first well region and a second well region of a second conductivity type opposite the first conductivity type are on the second side of the insulation region. A second HVW region of the first conductivity type is disposed between the first and the second well regions, wherein the second HVW region is connected to the buried well region. A source region of the first conductivity type is in a top surface region of the second HVW region, wherein the source region, the drain region, and the buried well region form a JFET.

[0031] In accordance with other embodiments, a device includes a substrate, a buried well region of a first conductivity type over the substrate, a HVW region of the first conductivity type over the buried well region, an insulation region over the HVW region, and a drain region of the first conductivity type on a first side of the insulation region and over the HVW region. A gate electrode includes a first portion on a second side of the insulation region, and a second portion extending over the insulation region. A source region of the first conductivity type is disposed over a first portion of the HVW region, wherein the source region, the drain region, and the buried well region form a JFET. A first, a second, and a third well region of a second conductivity type opposite the first conductivity type are disposed on the second side of the insulation region and interconnected to each other, wherein the first and the second well regions are spaced apart from each other by a second portion of the HVW region. The third well region is spaced apart from the first and the second well regions by the first portion of the HVW region.

[0032] In accordance with yet other embodiments, a device includes a substrate, a buried well region of a first conductivity type over the substrate, a HVW region of the first conductivity type over the buried well region, an insulation region over the HVW region, a drain region of the first conductivity type on a first side of the insulation region and over the HVW region, and a gate electrode having a first portion on a second side of the insulation region and a second portion extending over the insulation region. A well region of a second conductivity type opposite the first conductivity type is disposed on the second side of the insulation region. The well region includes a body, and a first leg and a second leg extending from the body toward the insulation region, wherein the body and the first and the second legs contact three edges of the HVW region. A source region of the first conductivity type is disposed over a portion of the HVW region, wherein the source region is between the first and the second legs of the well region, and wherein the source region, the drain region, and the buried well region form a JFET.

[0033] Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A method comprising:

conducting a current between a source region and a drain region of a Junction Field-Effect Transistor (JFET), wherein the current comprises:

a first portion underlying a first P-type Buried Layer (PBL), wherein the first portion of the current is further conducted through a first portion of an n-well region, with the n-well region between a first p-well region and a second p-well region; and

a second portion through a second portion of the n-well region, wherein the second portion of the n-well region is between the first PBL and a second PBL;